

**IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION**

COMPUTER CIRCUIT OPERATIONS LLC,

Plaintiff,

v.

SYNOPSYS, INC.,

Defendant.

Case No.: 6:21-cv-00139

Jury Trial Demanded

COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Computer Circuit Operations LLC (“CCO”) hereby files Complaint for patent infringement against Defendant Synopsys, Inc. (“Synopsys” or “Defendant”) and alleges as follows:

PARTIES

1. Plaintiff CCO is a limited liability company organized and existing under the laws of the State of New York, having its principal place of business at 1629 Sheepshead Bay Road, Floor 2, Brooklyn, New York, 11235.

2. On information and belief, Defendant Synopsys, Inc. is a corporation organized and existing under the laws of the State of Delaware.

JURISDICTION AND VENUE

3. This is an action under the patent laws of the United States, 35 U.S.C. §§ 1, et seq., for infringement by Synopsys of claims of U.S. Patent Nos. 6,480,021, 6,820,234, 7,107,386, 7,278,069, and 7,426,603 (“the Patents-in-Suit”).

4. This Court has subject matter jurisdiction pursuant to 28 U.S.C. §§ 1331 and

1338(a).

5. Synopsys is subject to personal jurisdiction of this Court because, inter alia, on information and belief, independently and/or via its agents, (i) Synopsys does business in Texas; (ii) Synopsys sells and offers for sale its products in Texas, (iii) Synopsys sells and offers for sale its products by using distributors and sales representatives located in Texas; and/or (iv) Synopsys places its products in the stream of commerce with intent or knowledge that those products would end up in Texas.

6. Venue is proper in this district under 28 U.S.C. § 1400(b) because (i) Synopsys has committed and continues to commit acts of patent infringement by, inter alia, offering for sale and selling, on their own and as part of a device, infringing Synopsys products; and (ii) has a regular and established place of business in this district, including at 4 Barton Skyway, 1301 S. MoPac Expressway, Suite 200, Austin, TX 78746.

BACKGROUND

7. On November 12, 2002, the United States Patent and Trademark Office duly and lawfully issued U.S. Patent No. 6,480,021 (“the ’021 Patent”), entitled “Transmitter Circuit Comprising Timing Deskewing Means.”

8. Alexander Roger Deas, Vasily Grigorievich Atyunin, and Igor Anatolievich Abrossimov, invented the technology claimed in the ’021 Patent.

9. On November 16, 2004, the United States Patent and Trademark Office duly and lawfully issued U.S. Patent No. 6,820,234 (“the ’234 Patent”), entitled “Skew Calibration Means And A Method Of Skew Calibration.”

10. Alexander Roger Deas, Ilya Valerievich Klotchkov, Igor Anatolievich Abrossimov, and Vasily Grigorievich Atyunin invented the technology claimed in the ’234

Patent.

11. On September 12, 2006, the United States Patent and Trademark Office duly and lawfully issued U.S. Patent No. 7,107,386 (“the ’386 Patent”), entitled “Memory Bus Arbitration Using Memory Bank Readiness.”

12. Stephen Clark Purcell and Scott Kimura invented the technology claimed in the ’386 Patent.

13. On October 2, 2007, the United States Patent and Trademark Office duly and lawfully issued U.S. Patent No. 7,278,069 (“the ’069 Patent”), entitled “Data Transmission Apparatus For High-Speed Transmission Of Digital Data and Method For Automatic Skew Calibration.”

14. Igor Anatolievich Abrosimov, Vasily Grigorievich Atyunin, Alexander Roger Deas, and Ilya Vasilievich Klotchkov invented the technology claimed in the ’069 Patent.

15. On September 16, 2008, the United States Patent and Trademark Office duly and lawfully issued U.S. Patent No. 7,426,603 (“the ’603 Patent”), entitled “Memory Bus Arbitration Using Memory Bank Readiness.”

16. Stephen Clark Purcell and Scott Kimura invented the technology of the ’603 Patent.

17. CCO is the assignee and owner of the right, title, and interest in and to the Patents-in-Suit, including the right to assert all causes of action arising under said patents and the right to any remedies for infringement.

NOTICE

18. By letter dated May 22, 2019, CCO notified Synopsys of the existence of the Patents-in-Suit, and of infringement of the ’234; ’386; ’069; and ’603 Patents by Synopsys.

CCO's letter identified exemplary infringing Synopsys products and an exemplary infringed claim for each of the '201,'234; '386; '069; and '603 Patents. CCO's May 22, 2019 letter invited Synopsys to hold a licensing discussion with CCO. As of the date of this Complaint, CCO has not received a response from Synopsys.

LICENSING

19. As of the time of this Complaint, CCO has entered into licensing agreements relating to the Patents-in-Suit with at least Arastu Systems, NVIDIA, Qualcomm, Via Technologies, Rockchip, and Socionext.

COUNT I: INFRINGEMENT OF THE '021 PATENT

20. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

21. On information and belief, Synopsys has infringed the '021 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States, or importing into the United States DDR3, DDR4, LPDDR3, and LPDDR4 memory controller systems ("DDR Controller") individually or as part of a processor or System-on-Chip (collectively, "Accused Synopsys Products").

22. On information and belief, Synopsys has infringed at least claim 11 of the '021 Patent by performing a method of eliminating skew caused by inter-symbol interference and cross-talk influence in the transmission line for high-speed transmission of digital data by modifying delays at each DQ line of an exemplary DDR Controller, such as an LPDDR4/LPDDR4x Controller incorporated in the Accused Synopsys Products, including during regular operation and during development, design, testing, and verification of the DDR Controller, in part because they operate in compliance with LPDDR4 JEDEC standard. Ex. 16 (blogs.synopsys.com website); Ex. 1 at 25, 27, 237 (DesignWare Cores LPDDR4x multiPHY

Utility Block (PUB) Databook, Synopsys, Jun. 2018); Ex. 5 at 195 (JEDEC Standard, LPDDR4, JESD209-4B, Feb. 2017); Ex. 19 (intel.cn website).

23. On information and belief, the Synopsys DDR Controller continuously transmits data through each transmission line, such as DQ transmission line, provided by at least one driver. Ex. 1 at 192, 392, 437 (DesignWare Cores LPDDR4x multiPHY Utility Block (PUB) Databook, Synopsys, Jun. 2018); Ex. 5 at 195 (JEDEC Standard, LPDDR4, JESD209-4B, Feb. 2017); Ex. 10 at 67 (C. Kim et al., High-Bandwidth Memory Interface).

24. On information and belief, the Synopsys DDR Controller measures a skew for the transmitted DQ bit patterns by training write boundaries of a data eye during write leveling. Ex. 16 (blogs.synopsys.com website); Ex. 1 at 39, 237 (DesignWare Cores LPDDR4x multiPHY Utility Block (PUB) Databook, Synopsys, Jun. 2018); Ex. 5 at 195 (JEDEC Standard, LPDDR4, JESD209-4B, Feb. 2017).

25. On information and belief, the Synopsys DDR Controller records and stores information on skew caused by inter-symbol interference and cross-talk influence in the DQ transmission lines for at least one data pattern transmitted through the transmission line. Ex. 16 (blogs.synopsys.com website); Ex. 5 at 195 (JEDEC Standard, LPDDR4, JESD209-4B, Feb. 2017); Ex. 19 (intel.cn website).

26. On information and belief, the Synopsys DDR Controller generates and applies a correction to the timing position of a signal transition between two logical levels, the correction being generated on the basis of the information stored in the storage means, so as to compensate for the above skew. Ex. 16 (blogs.synopsys.com website); Ex. 5 at 195, 200 (JEDEC Standard, LPDDR4, JESD209-4B, Feb. 2017).

27. On information and belief, Synopsys has induced, and continues to induce,

infringement of the '021 Patent pursuant to 35 U.S.C. § 271(b), by actively and knowingly inducing, directing, causing, and encouraging others, including, but not limited to, its customers and end users, to make, use, sell, and/or offer to sell in the United States, and/or import into the United States, the Accused Synopsys Products that incorporate the DDR Controller. Synopsys had the knowledge of the '021 Patent, at least from the time of receiving CCO's May 22, 2019, notice of infringement, and acted with specific intent to encourage its customers and end users to make, use, sell, and/or offer to sell in the United States and/or import into the United States the infringing instrumentalities described above, including by providing the DDR Controller, corresponding technical documentation, and assisting customers with integrating, testing, and verification thereof.

28. On information and belief, Synopsys has committed the foregoing infringing activities without a license.

29. On information and belief, Synopsys' infringing activities commenced within six years prior to the filing of this complaint, entitling CCO to past damages.

COUNT II: INFRINGEMENT OF THE '234 PATENT

30. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

31. On information and belief, Synopsys has infringed the '234 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States, or importing into the United States the Accused Synopsys Products.

32. For example, on information and belief, Synopsys has infringed at least claim 28 of the '234 Patent by making, using, offering to sell, selling in the United States, or importing into the United States the Accused Synopsys Products that include the DDR Controller, such as DDR3, DDR3L, DDR4, LPDDR3, LPDDR4, and LPDDR4x Memory Controller Systems, with

a timing uncertainty reduction system for calibration of a high speed communication apparatus, including during development, design, testing, and verification of the Accused Synopsys Products and specifically the DDR Controller. Ex. 13 (synopsys.com website); Ex. 1 at 20, 24-25 (DesignWare Cores LPDDR4x multiPHY Utility Block (PUB) Databook, Synopsys, Jun. 2018); Ex. 16 (blogs.synopsys.com).

33. On information and belief, an exemplary DDR Controller reduces timing uncertainty in DDR3, DDR3L, DDR4, LPDDR3, LPDDR4, and LPDDR4x memory transmission including calibration using the Multi-Purpose Register (MPR), read centering, write centering, and write leveling. Ex. 7 at 8, 31, 37 (JEDEC Standard, DDR4 SDRAM, JESD79-4, Sept. 2012); Ex. 18 (systemverilog.io); Ex. 6 at 17, 42, 48-51 (JEDEC Standard, DDR3 SDRAM, JESD79-3C, Nov. 2008); Ex. 5 at 26, 190, 195 (JEDEC Standard, LPDDR4, JESD209-4B, Feb. 2017); Ex. 4 at 61, 68 (JEDEC Standard, LPDDR3, JESD209-3C, Aug. 2015); Ex. 9 at 55 (DDR PHY Interface, DFI 4.0 Specification).

34. On information and belief, the DDR Controller comprises at least one driving register for latching transmitted DQ signals, with a plurality of inputs and outputs. Ex. 1 at 392 (DesignWare Cores LPDDR4x multiPHY Utility Block (PUB) Databook, Synopsys, Jun. 2018); Ex. 2 at 36 (DesignWare Cores DDR multiPHY Databook for SMIC40LL25, Synopsys, Jul. 2011); Ex. 10 at 67 (C. Kim et al., High-Bandwidth Memory Interface).

35. On information and belief, the DDR Controller further comprises at least one receiving register for latching received DQ signals, with a plurality of inputs and outputs. Ex. 2 at 89, 91-92 (DesignWare Cores DDR multiPHY Databook for SMIC40LL25, Synopsys, Jul. 2011); Ex. 1 at 373 (DesignWare Cores LPDDR4x multiPHY Utility Block (PUB) Databook, Synopsys, Jun. 2018); Ex. 11 at 13, 19-20 (Technical Note, High-Speed DRAM Controller

Design, Micron); Ex. 10 at 67 (C. Kim et al., High-Bandwidth Memory Interface).

36. On information and belief, the DDR Controller includes a main clock (such as a PLL or DLL) for generating a main clock signal. Ex. 2 at 24, 61, 89 (DesignWare Cores DDR multiPHY Databook for SMIC40LL25, Synopsys, Jul. 2011).

37. On information and belief, the DDR Controller includes a reference clock, such as an internal clock or a DLL clock, for generating a reference signal for calibrating the receiving register or registers, such as during DQ read centering/read training; said reference clock being associated with the main clock signal. Ex. 2 at 38, 89 (DesignWare Cores DDR multiPHY Databook for SMIC40LL25, Synopsys, Jul. 2011); Ex. 11 at 19-20 (Technical Note, High-Speed DRAM Controller Design, Micron); Ex. 9 at 147 (DDR PHY Interface, DFI 4.0 Specification); Ex. 8 at 117-118 (DDR PHY Interface, DFI 3.1 Specification, Version 3.1); Ex. 18 (systemverilog.io website); Ex. 6 at 48-51 (JEDEC Standard, DDR3 SDRAM, JESD79-3C, Nov. 2008); Ex. 5 at 190, 190 (JEDEC Standard, LPDDR4, JESD209-4B, Feb. 2017); Ex. 4 at 61 (JEDEC Standard, LPDDR3, JESD209-3C, Aug. 2015).

38. On information and belief, the DDR Controller includes phase shift circuitry to align the timing of the driving signals' relative to the CK signal at the destination, such as phase shift circuitry aligning the timing of the DQS signals via write leveling, or DQ signals following write centering. Ex. 2 at 18 (DesignWare Cores DDR multiPHY Databook for SMIC40LL25, Synopsys, Jul. 2011); Ex. 1 at 25, 185 (DesignWare Cores LPDDR4x multiPHY Utility Block (PUB) Databook, Synopsys, Jun. 2018); Ex. 16 (blogs.synopsys.com website); Ex. 18 (systemverilog.io website); Ex. 7 at 31-33 (JEDEC Standard, DDR4 SDRAM, JESD79-4, Sept. 2012); Ex. 6 at 42-43 (JEDEC Standard, DDR3 SDRAM, JESD79-3C, Nov. 2008); Ex. 5 at 186, 195 (JEDEC Standard, LPDDR4, JESD209-4B, Feb. 2017); Ex. 4 at 61, 68 (JEDEC Standard,

LPDDR3, JESD209-3C, Aug. 2015).

39. On information and belief, Synopsys has induced, and continues to induce, infringement of the '234 Patent pursuant to 35 U.S.C. § 271(b), by actively and knowingly inducing, directing, causing, and encouraging others, including, but not limited to, its customers and end users, to make, use, sell, and/or offer to sell in the United States, and/or import into the United States, the Accused Synopsys Products that incorporate the DDR Controller. Synopsys had the knowledge of the '234 Patent, at least from the time of receiving CCO's May 22, 2019, notice of infringement, and acted with specific intent to encourage its customers and end users to make, use, sell, and/or offer to sell in the United States and/or import into the United States the infringing instrumentalities described above, including by providing the DDR Controller, corresponding technical documentation, and assisting customers with integrating, testing, and verification thereof.

40. On information and belief, Synopsys has committed the foregoing infringing activities without a license.

41. On information and belief, Synopsys' infringing activities commenced within six years prior to the filing of this complaint, entitling CCO to past damages.

42. On information and belief, Synopsys knew the '234 Patent existed, knew of its claims, and knew of Synopsys' infringing products while committing the foregoing infringing acts, thereby willfully, wantonly, and deliberately infringing the '234 Patent.

COUNT III: INFRINGEMENT OF THE '386 PATENT

43. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

44. On information and belief, Synopsys has infringed the '386 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell,

selling in the United States or importing into the United States the Accused Synopsys Products.

45. For example, on information and belief, Synopsys has infringed at least claim 1 of the '386 Patent by making, using, offering to sell, selling in the United States or importing into the United States the Accused Synopsys Products, which include a DDR Controller, such as DDR3, DDR3L, DDR4, LPDDR2, LPDDR3, LPDDR4, and LPDDR4x Memory Controller Systems, adapted to send a plurality of memory transactions over a memory bus to a memory having a plurality of memory banks. Ex. 17 (archive.eetasia.com website); Ex. 14 (synopsys.com website); Ex. 1 at 113, 177 (DesignWare Cores LPDDR4x multiPHY Utility Block (PUB) Databook, Synopsys, Jun. 2018); Ex. 15 (synopsys.com website); Ex. 6 at 15-16 (JEDEC Standard, DDR3 SDRAM, JESD79-3C, Nov. 2008); Ex. 7 at 7 (JEDEC Standard, DDR4 SDRAM, JESD79-4, Sept. 2012); Ex. 3 at 12 (JEDEC Standard, LPDDR2, JESD209-2B, Feb. 2010); Ex. 4 at 16 (JEDEC Standard, LPDDR3, JESD209-3C, Aug. 2015); Ex. 5 at 19 (JEDEC Standard, LPDDR4, JESD209-4B, Feb. 2017).

46. On information and belief, the DDR Controller comprises a queue comprising a plurality of request stations, wherein each of the plurality of memory transactions is stored in one of the request stations and is addressed to one of the plurality of memory banks. Ex. 14 (synopsys.com website); Ex. 6 at 33 (JEDEC Standard, DDR3 SDRAM, JESD79-3C, Nov. 2008); Ex. 7 at 24 (JEDEC Standard, DDR4 SDRAM, JESD79-4, Sept. 2012); Ex. 3 at 145 (JEDEC Standard, LPDDR2, JESD209-2B, Feb. 2010); Ex. 4 at 80 (JEDEC Standard, LPDDR3, JESD209-3C, Aug. 2015); Ex. 5 at 246 (JEDEC Standard, LPDDR4, JESD209-4B, Feb. 2017).

47. On information and belief, the DDR Controller includes an arbiter, such as the Command Scheduler, coupled to each of the plurality of request stations, adapted to select any of the plurality of memory transactions. Ex. 14 (synopsys.com website).

48. On information and belief, the arbiter of the DDR Controller is configured to generate a plurality of bank readiness signals, each bank readiness signal indicating the readiness of one of the plurality of memory banks to accept a memory transaction, and, based on the bank readiness signals, is configured to select one of the memory transactions for transmission over the memory bus. *Id.*; Ex. 6 at 55 (JEDEC Standard, DDR3 SDRAM, JESD79-3C, Nov. 2008); Ex. 7 at 9, 82 (JEDEC Standard, DDR4 SDRAM, JESD79-4, Sept. 2012); Ex. 3 at 18, 79 (JEDEC Standard, LPDDR2, JESD209-2B, Feb. 2010); Ex. 4 at 16, 35 (JEDEC Standard, LPDDR3, JESD209-3C, Aug. 2015); Ex. 5 at 18, 58 (JEDEC Standard, LPDDR4, JESD209-4B, Feb. 2017); Ex. 6 at 18 (JEDEC Standard, DDR3 SDRAM, JESD79-3C, Nov. 2008).

49. On information and belief, Synopsys has induced, and continues to induce, infringement of the '386 Patent pursuant to 35 U.S.C. § 271(b), by actively and knowingly inducing, directing, causing, and encouraging others, including, but not limited to, its customers and end users, to make, use, sell, and/or offer to sell in the United States, and/or import into the United States the DDR Controller. Synopsys had the knowledge of the '386 Patent, at least from the time of receiving CCO's May 22, 2019, notice of infringement, and acted with specific intent to encourage its customers and end users to make, use, sell, and/or offer to sell in the United States and/or import into the United States the infringing instrumentalities described above, including by providing the DDR Controller, corresponding technical documentation, and assisting customers with integrating, testing, and verification thereof.

50. On information and belief, Synopsys has committed the foregoing infringing activities without a license.

51. On information and belief, Synopsys' infringing activities commenced within six years prior to the filing of this complaint, entitling CCO to past damages.

52. On information and belief, Synopsys knew the '386 Patent existed, knew of its claims, and knew of Synopsys infringing products while committing the foregoing infringing acts, thereby willfully, wantonly, and deliberately infringing the '386 Patent.

COUNT IV: INFRINGEMENT OF THE '069 PATENT

53. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

54. On information and belief, Synopsys has infringed the '069 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell, selling in the United States, or importing into the United States the Accused Synopsys Products.

55. For example, on information and belief, Synopsys has infringed at least claim 12 of the '069 Patent by performing a method for automatic skew calibration of a transmission apparatus for high speed transmission of digital data, comprising a transmitter and a receiver, including during development, design, testing, and verification of the Accused Synopsys Products, which include the DDR Controller, such as a DDR3, DDR3L, DDR4, LPDDR3, LPDDR4 and LPDDR4x memory controllers that automatically calibrate skew. Ex. 1 at 20-21, 24-25 (DesignWare Cores LPDDR4x multiPHY Utility Block (PUB) Databook, Synopsys, Jun. 2018); Ex. 13 (synopsys.com website); Ex. 10 at 67 (C. Kim et al., High-Bandwidth Memory Interface); Ex. 9 at 18-19 (DDR PHY Interface, DFI 4.0 Specification).

56. The DDR Controller calibrates registers of the receiver in relation to a reference clock edge. Ex. 1 at 38, 89, 91, 133, 185, 194 (DesignWare Cores LPDDR4x multiPHY Utility Block (PUB) Databook, Synopsys, Jun. 2018); Ex. 9 at 16, 147 (DDR PHY Interface, DFI 4.0 Specification); Ex. 11 at 19-20 (Technical Note, High-Speed DRAM Controller Design, Micron).

57. The DDR Controller calibrates propagation delays of registers of the transmitter,

using the calibrated registers of the receiver, such as the registers calibrated to receive the samples of CK_t – CK_c during write leveling. Ex. 1 at 25, 27-28 (DesignWare Cores LPDDR4x multiPHY Utility Block (PUB) Databook, Synopsys, Jun. 2018); Ex. 16 (blogs.synopsys.com); Ex. 9 at 57, 146-147, 190 (DDR PHY Interface, DFI 4.0 Specification); Ex. 7 at 31 (JEDEC Standard, DDR4 SDRAM, JESD79-4, Sept. 2012); Ex. 6 at 42 (JEDEC Standard, DDR3 SDRAM, JESD79-3C, Nov. 2008); Ex. 5 at 186 (JEDEC Standard, LPDDR4, JESD209-4B, Feb. 2017); Ex. 4 at 68 (JEDEC Standard, LPDDR3, JESD209-3C, Aug. 2015); Ex. 18 (systemverilog.io website).

58. On information and belief, the DDR Controller's calibration is performed by measuring time offsets between different signals that form a communication channel. Ex. 16 (blogs.synopsys.com website); Ex. 7 at 30-31, 33 (JEDEC Standard, DDR4 SDRAM, JESD79-4, Sept. 2012); Ex. 1 at 21, 27-28, 133 (DesignWare Cores LPDDR4x multiPHY Utility Block (PUB) Databook, Synopsys, Jun. 2018); Ex. 6 at 40, 42-43 (JEDEC Standard, DDR3 SDRAM, JESD79-3C, Nov. 2008); Ex. 16 (blogs.synopsys.com website); Ex. 5 at 186, 244 (JEDEC Standard, LPDDR4, JESD209-4B, Feb. 2017); Ex. 4 at 68, 78 (JEDEC Standard, LPDDR3, JESD209-3C, Aug. 2015); Ex. 18 (systemverilog.io website); Ex. 9 at 190 (DDR PHY Interface, DFI 4.0 Specification).

59. On information and belief, the DDR Controller applies the measured time offsets to compensate for the inter-signal skew by performing relative alignment of the measured offsets to a main clock edge. Ex. 1 at 25, 36-38 (DesignWare Cores LPDDR4x multiPHY Utility Block (PUB) Databook, Synopsys, Jun. 2018); Ex. 7 at 32-33 (JEDEC Standard, DDR4 SDRAM, JESD79-4, Sept. 2012); Ex. 6 at 42-43 (JEDEC Standard, DDR3 SDRAM, JESD79-3C, Nov. 2008); Ex. 5 at 186 (JEDEC Standard, LPDDR4, JESD209-4B, Feb. 2017); Ex. 4 at 68 (JEDEC

Standard, LPDDR3, JESD209-3C, Aug. 2015).

60. On information and belief, Synopsys has induced, and continues to induce, infringement of the '069 Patent pursuant to 35 U.S.C. § 271(b), by actively and knowingly inducing, directing, causing, and encouraging others, including, but not limited to, its customers and end users, to make, use, sell, and/or offer to sell in the United States, and/or import into the United States, the Accused Synopsys Products that incorporate the DDR Controller. Synopsys had the knowledge of the '069 Patent, at least from the time of receiving CCO's May 22, 2019, notice of infringement, and acted with specific intent to encourage its customers and end users to make, use, sell, and/or offer to sell in the United States and/or import into the United States the infringing instrumentalities described above, including by providing the DDR Controller, corresponding technical documentation, and assisting customers with integrating, testing, and verification thereof.

61. On information and belief, Synopsys has committed the foregoing infringing activities without a license.

62. On information and belief, Synopsys' infringing activities commenced within six years prior to the filing of this complaint, entitling CCO to past damages.

63. On information and belief, Synopsys knew the '069 Patent existed, knew of its claims, and knew of Synopsys infringing products while committing the foregoing infringing acts, thereby willfully, wantonly, and deliberately infringing the '069 Patent.

COUNT V: INFRINGEMENT OF THE '603 PATENT

64. Plaintiff incorporates the preceding paragraphs as if fully set forth herein.

65. On information and belief, Synopsys has infringed the '603 Patent pursuant to 35 U.S.C. § 271(a), literally or under the doctrine of equivalents, by making, using, offering to sell,

selling in the United States or importing into the United States the Accused Synopsys Products.

66. For example, on information and belief, Synopsys' Systems-on-Chips infringed at least claim 16 of the '603 Patent by performing a method of using a multiplexer to manage the transmission of a plurality of memory transactions to a memory having a plurality of memory banks, including during development, design, testing, and verification of the DDR Controllers, such as a DDR3, DDR3L, DDR4, LPDDR2, LPDDR3, LPDDR4 and LPDDR4x. Ex. 14 (synopsys.com website); Ex. 15 (synopsys.com website); Ex. 6 at 15 (JEDEC Standard, DDR3 SDRAM, JESD79-3C, Nov. 2008); Ex. 7 at 7 (JEDEC Standard, DDR4 SDRAM, JESD79-4, Sept. 2012); Ex. 3 at 12 (JEDEC Standard, LPDDR2, JESD209-2B, Feb. 2010); Ex. 4 at 16 (JEDEC Standard, LPDDR3, JESD209-3C, Aug. 2015); Ex. 5 at 19 (JEDEC Standard, LPDDR4, JESD209-4B, Feb. 2017).

67. On information and belief, the multiplexer used by the Synopsys DDR Controller comprises a plurality of multiplexer inputs for receiving the plurality of memory transactions and a multiplexer output for sending each of the plurality of memory transactions to the memory. *Id.*

68. On information and belief, the Synopsys DDR Controller receives a plurality of memory transactions at the multiplexer inputs, wherein each memory transaction is addressed to a corresponding memory bank, in accordance with the respective JEDEC standards for each DDR Controller. Ex. 14 (synopsys.com website); Ex. 6 at 33 (JEDEC Standard, DDR3 SDRAM, JESD79-3C, Nov. 2008); Ex. 7 at 24 (JEDEC Standard, DDR4 SDRAM, JESD79-4, Sept. 2012); Ex. 3 at 145 (JEDEC Standard, LPDDR2, JESD209-2B, Feb. 2010); Ex. 4 at 80 (JEDEC Standard, LPDDR3, JESD209-3C, Aug. 2015); Ex. 5 at 246 (JEDEC Standard, LPDDR4, JESD209-4B, Feb. 2017).

69. On information and belief, the Synopsys DDR Controller associates a priority

with each received memory transaction. Ex. 14 (synopsys.com website).

70. On information and belief, the DDR Controller generates a plurality of bank readiness signals indicating the readiness of each memory bank available to accept a memory transaction, wherein the plurality of bank readiness signals are based on the plurality of memory transactions at the multiplexer inputs and the multiplexer output, in accordance with the respective JEDEC standards for each DDR Controller. *Id.*; Ex. 6 at 55 (JEDEC Standard, DDR3 SDRAM, JESD79-3C, Nov. 2008); Ex. 7 at 82 (JEDEC Standard, DDR4 SDRAM, JESD79-4, Sept. 2012); Ex. 3 at 79 (JEDEC Standard, LPDDR2, JESD209-2B, Feb. 2010); Ex. 4 at 35 (JEDEC Standard, LPDDR3, JESD209-3C, Aug. 2015); Ex. 5 at 58 (JEDEC Standard, LPDDR4, JESD209-4B, Feb. 2017); Ex. 6 at 18 (JEDEC Standard, DDR3 SDRAM, JESD79-3C, Nov. 2008); Ex. 7 at 9 (JEDEC Standard, DDR4 SDRAM, JESD79-4, Sept. 2012); Ex. 3 at 18 (JEDEC Standard, LPDDR2, JESD209-2B, Feb. 2010); Ex. 4 at 16 (JEDEC Standard, LPDDR3, JESD209-3C, Aug. 2015); Ex. 5 at 18 (JEDEC Standard, LPDDR4, JESD209-4B, Feb. 2017).

71. On information and belief, the Synopsys DDR Controller sends each of the plurality of memory transactions to its corresponding memory banks via the multiplexer output based on the associated priorities and the bank readiness signals. Ex. 14 (synopsys.com website).

72. On information and belief, the Synopsys DDR Controller prioritizes each memory transaction based on the memory transaction's position in a queue. Ex. 14 (synopsys.com website).

73. On information and belief, Synopsys has induced, and continues to induce, infringement of the '603 Patent pursuant to 35 U.S.C. § 271(b), by actively and knowingly

inducing, directing, causing, and encouraging others, including, but not limited to, its customers and end users, to make, use, sell, and/or offer to sell in the United States, and/or import into the United States the DDR Controller. Synopsys had the knowledge of the '603 Patent, at least from the time of receiving CCO's May 22, 2019, notice of infringement, and acted with specific intent to encourage its customers and end users to make, use, sell, and/or offer to sell in the United States and/or import into the United States the infringing instrumentalities described above, including by providing the DDR Controller, corresponding technical documentation, and assisting customers with integrating, testing, and verification thereof.

74. On information and belief, Synopsys has committed the foregoing infringing activities without a license.

75. On information and belief, Synopsys' infringing activities commenced within six years prior to the filing of this complaint, entitling CCO to past damages.

76. On information and belief, Synopsys knew the '603 Patent existed, knew of its claims, and knew of Synopsys' infringing products while committing the foregoing infringing acts, thereby willfully, wantonly, and deliberately infringing the '603 Patent.

PRAYER FOR RELIEF

WHEREFORE, Plaintiff CCO prays for the judgment in its favor against Synopsys, and specifically, for the following relief:

- A. Entry of judgment in favor of CCO against Synopsys on all counts;
- B. Entry of judgment that Synopsys has infringed the Patents-in-Suit;
- C. Entry of judgment that Synopsys' infringement of the '021, '234, '386, '069; and '603 Patents has been willful;
- D. An order permanently enjoining Synopsys from infringing the Patents-in-Suit;

- E. Award of compensatory damages adequate to compensate CCO for Synopsys' infringement of the Patent-in-Suit, in no event less than a reasonable royalty trebled as provided by 35 U.S.C. § 284;
- F. Award of CCO's costs;
- G. Pre-judgment and post-judgment interest on CCO's award; and
- H. All such other and further relief as the Court deems just or equitable.

DEMAND FOR JURY TRIAL

Pursuant to Rule 38 of the Fed. R. Civ. P., Plaintiff CCO hereby demands trial by jury in this action of all claims so triable.

Respectfully Submitted,

February 9, 2021

By: /s/ Raymond W. Mort, III

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